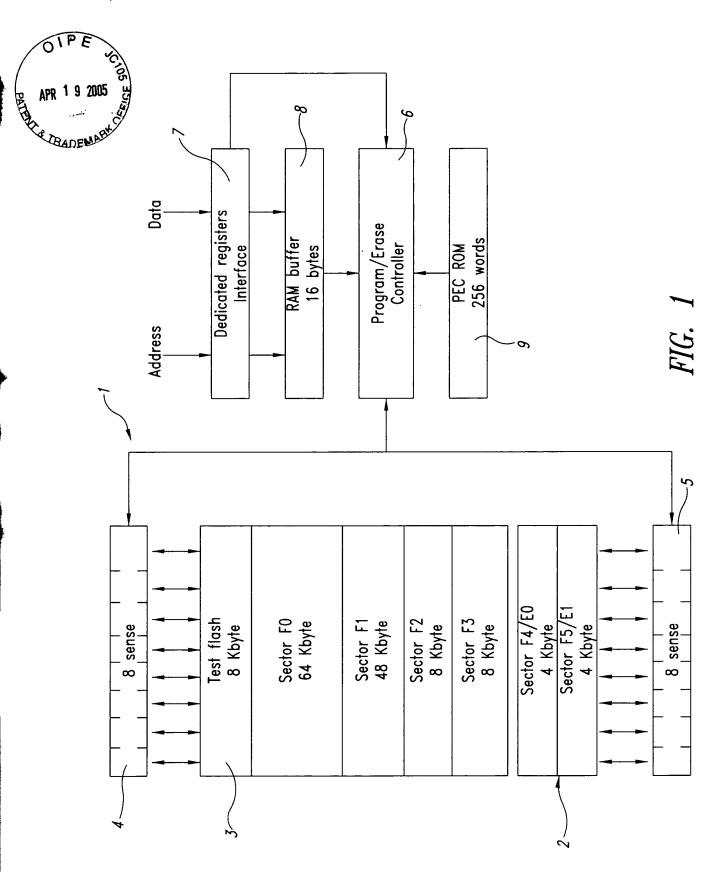
Serial No. 09/265,119 Docket No. 856063.579
Inventor(s): Maurizio Peri et al.
Express Mail No. EV335614719US "REPLACEMENT SHEET"



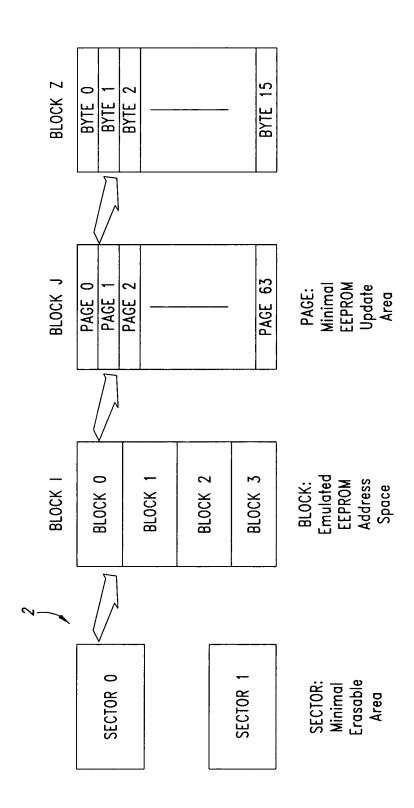


FIG. 2

on sector 0 done Erase phase 0 Erase phase 3 on sector 1 done sector 1 ready on sector 1 done Erase phase 2 Simplification: 4 pages (instead of 64) for each block on sector 1 done Erase phase 1 on sector 1 done Erase phase 0 block 3 block 0 block 0 block 1 block 2 block 1 block block EEPROM sector 0 sector 1 **EEPROM**

FIG. 5

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224000h	FCR
224001h	ECR
224002h	FSR

FIG. 3A

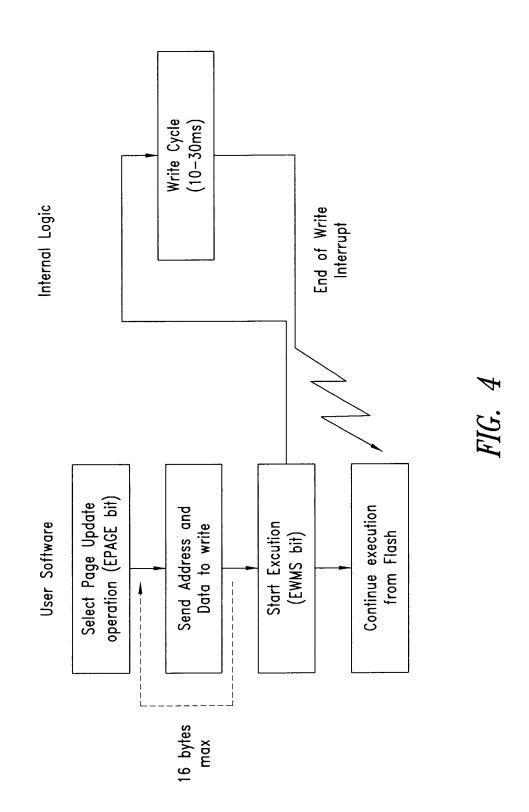
Sector	Addresses	Max Size
ОТР	211F80h to 211FFFh	128 byte
Flash 0	000000h to 00FFFFh	64 Kbyte
Flash 1	01000h to 01BFFFh	48 Kbyte
Flash 2	01C000h to 01DFFFh	8 Kbyte
Flash 3	01E000h to 01FFFFh	8 Kbyte
EEprom	220000h to 2203FFh	1 Kbyte

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		1					-
0	FBUSY		0	EBUSY	0	FSS0	
1	PROT		-	FEIEN		FSS1	
2	FSUSP		2	WFIS	2	FSS2	
3	FSECT	FIG. 3C	3		FIG. 3D	FSS3	1
4	FBYTE		4		FIG.	FSS4	1
5	FCHIP	ı	S.	ECHIP	ın	FSS5	
9	FPAGE	•	و	EPAGE	ဖ	FSS6	
7	FWMS	r	,	EWMS	7	FERR	

FIG. 3E

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211FFCh	NVAPR
211FFDh	NVWPR
211FFEh	NVPWD0
211FFFh	NVPWD1

FIG. 4A

Operation	Size	Min	Тур	Max
Page Update	256 byte	160 us	10 ms	30 ms
	512 byte	160 us	15 ms	50 ms
	1 Kbyte	160 us	30ms	100 ms
Chip Erase	256 byte		35 ms	100 ms
	512 byte		45 ms	150 ms
	1 Kbyte		70 ms	300 ms

FIG. 4B

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		1					
0	PWT0		0	WPRS0		0	PWD0
-	PWT1		1	WPRS1		-	PWD1
2	PWT2		2	WPRS2		2	PWD2
3	APEX	FIG. 4C	3	WPRS3	FIG. 4D	23	PWD3
4	APEE	FIG	4	WPEE	FIG	4	PWD4
5	APBR		5	WPBR		ഹ	PWD5
9	APRO		9	PWOK		9	PWD6
7	APRA		7	TMDIS		7	PWD7

FIG. 4E

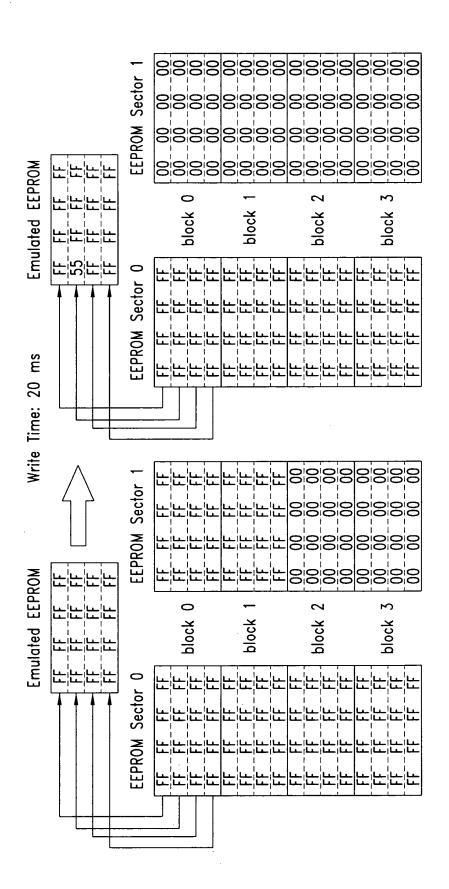


FIG. 5

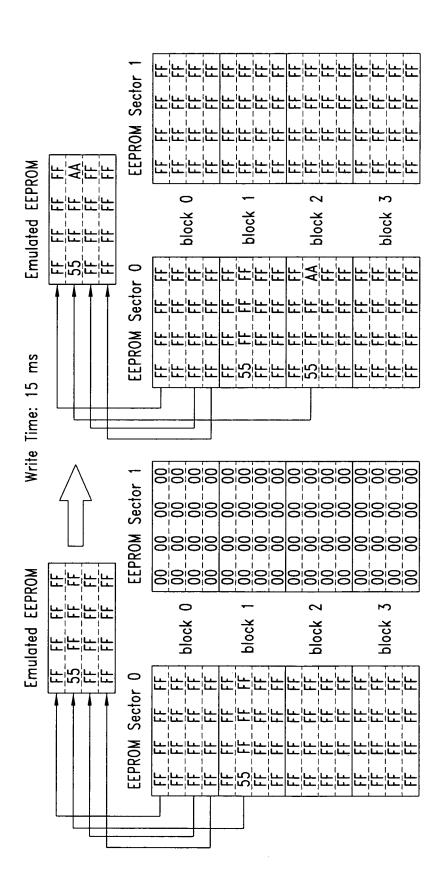


FIG. 6

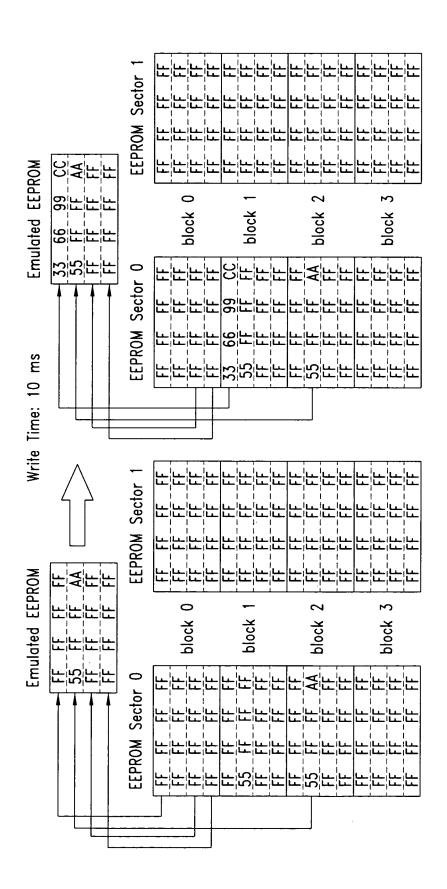


FIG. 7

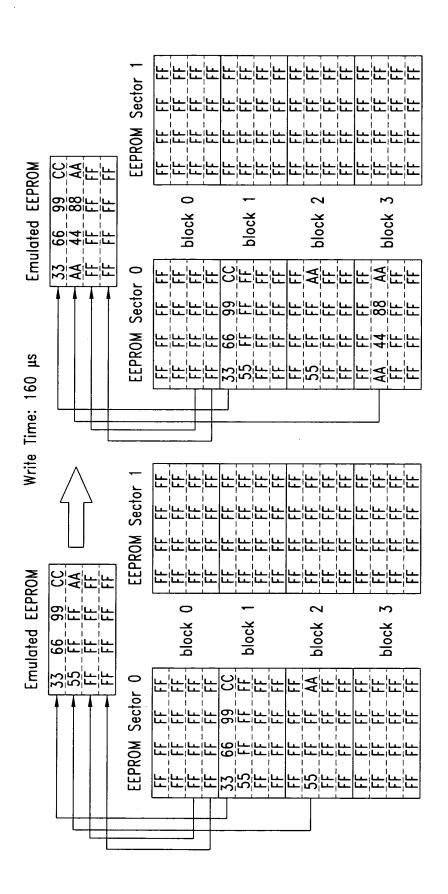


FIG. 8

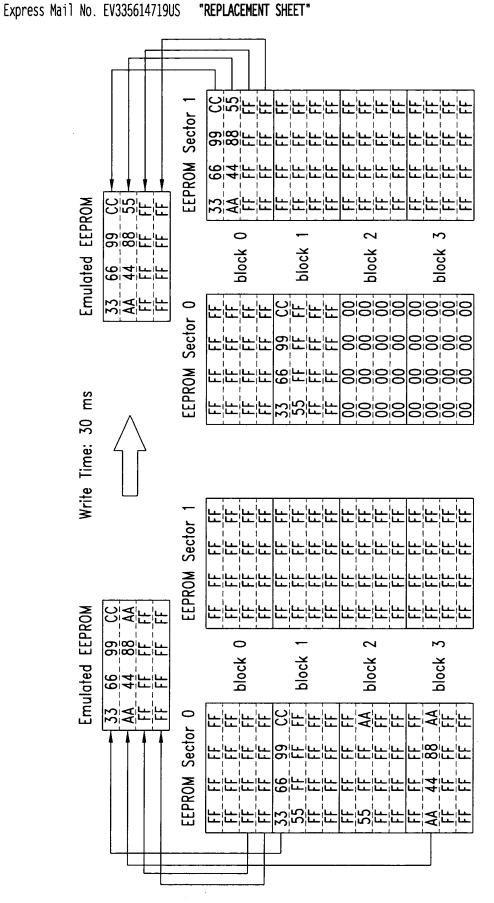


FIG. 9

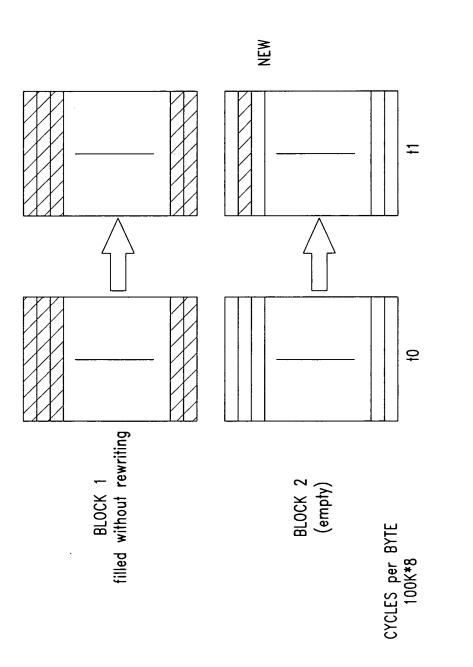
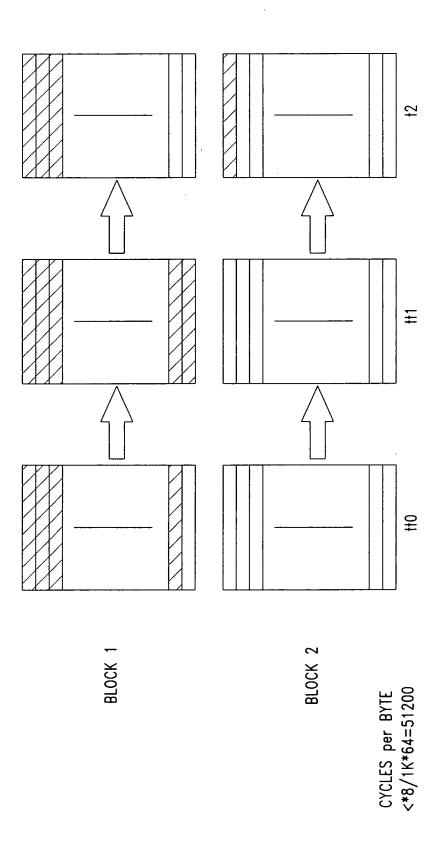


FIG. 10

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2 BLOCK 2 BLOCK 3

CYCLES per BYTE 100K*8/1K=800

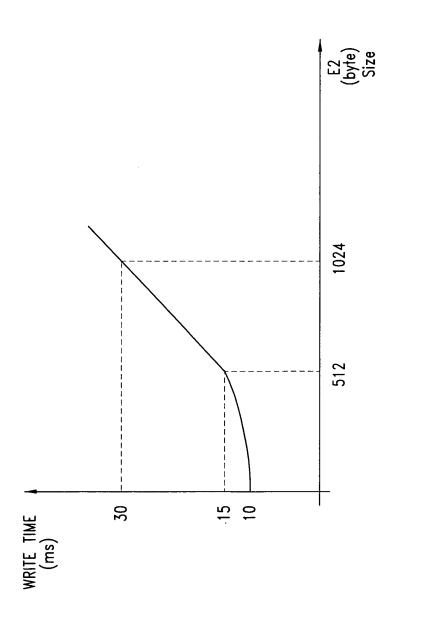


FIG. 13

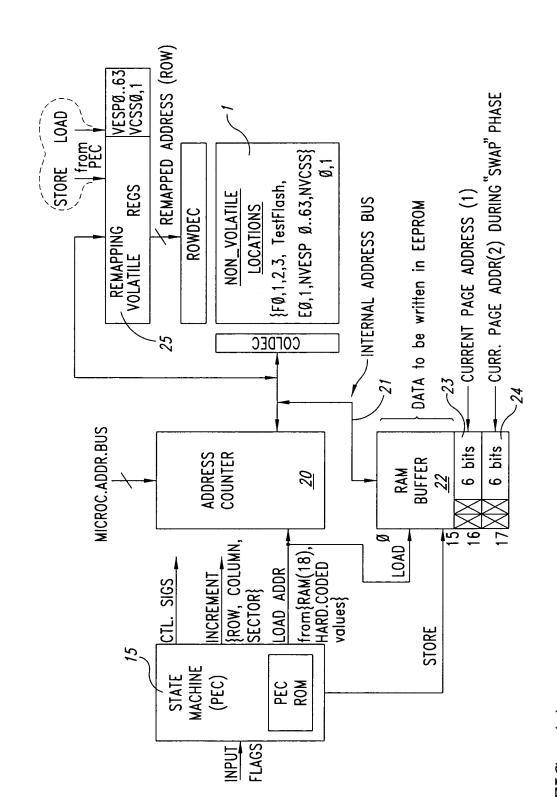


FIG. 14